MEMORY MAPPING FOR

PARALLEL TURBO DECODING

ABSTRACT OF THE DISCLOSURE

A routing multiplexer system provide p outputs
5   based on a selected permutation of p inputs. Each of
a plurality of modules has two inputs, two outputs
and a control input and is arranged to supply signals
at the two inputs to the two outputs in a direct or
transposed order based on a value of a bit at the
10   control input. A first p/2 group of the modules are
coupled to the n inputs and a second p/2 group of the
modules provide the n outputs. A plurality of
control bit tables each contains a plurality of bits
in an arrangement based on a respective permutation.
15   The memory is responsive to a selected permutation to
supply bits to the respective modules based on
respective bit values of a respective control bit
table,   thereby   establishing   a   selected   and
programmable permutation of the inputs to the
20   outputs.